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Title: ***Exploring Emerging Technologies in the HPC Co-Design Space***

Abstract:

Recent trends in HPC have forced our community to reexamine the full spectrum of architectures, software, and applications that constitute our HPC ecosystem. Architectural trends, such as heterogeneous processing and nonvolatile memory, are emerging in response to concerns about energy-efficiency and reliability. Meanwhile, applications are being redesigned so that they achieve new scientific objectives, expose prodigious amounts of hierarchical parallelism, and carefully orchestrate data movement. In what we have termed 'co-design,' teams of architects, software designers, and applications scientists, are working collectively to realize an integrated solution. Not surprisingly, this design space can be massive, uncertain, and discontinuous. To assist in this design space exploration, our team has recently developed a number of techniques for modeling, simulating, and measuring these future systems in order to predict performance, power, and reliability. For example, our Aspen (Abstract Scalable Performance Engineering Notation) performance modeling language allows users to compose and solve arbitrary performance modeling questions quickly and rigorously when compared to the traditional manual approach.